[0094] In many embodiments, a cap is only in the gate region and not in the access region. However, in other embodiments, the cap extends across the access region as well.

[0095] Reference is made to fluorine treatment throughout the specification. This treatment may result in fluorine doping in the semiconductor layers.

[0096] Many intermediary structures are described herein, which are subsequently finished by depositing a gate metal and source and drain ohmic contacts. Further, individual devices can be isolated when multiple devices are formed on a single substrate. Where these steps are not explicitly stated, it is assumed that one would finish the device using known techniques.

[0097] The transistors described herein are power transistors, which are capable of blocking at least 600 V, such as at least 900 V or at least 1200 V.

[0098] A number of embodiments of the invention have been described. Nevertheless, it will be understood that various modifications may be made without departing from the spirit and scope of the invention. For example, many of the features described with one embodiment may be used with another embodiment. Accordingly, other embodiments are within the scope of the following claims.

What is claimed is:

1. A method of forming an N-face enhancement mode high electron mobility transistor device, comprising:
- forming on a substrate a Ga-faced sacrificial layer;
- forming a cap layer on the sacrificial layer;
- forming a GaN channel layer on the cap layer;
- forming an Al_xGaN layer on the channel layer, wherein $0 \leqq x \leqq 1$;
- forming a buffer layer on the Al_xGaN layer;
- bonding a carrier wafer on the buffer layer to form a stack;
- removing the substrate and the sacrificial layer from the stack to form an N-faced assembly of layers; and
- forming a gate, source and drain on the N-faced assembly of layers.

2. The method of claim **1**, wherein forming a GaN channel layer on the cap layer comprises forming a channel layer of GaN with up to 15% Al in the GaN.

3. The method of claim **1**, wherein the cap layer comprises p-type Al_zGaN and the method further comprises etching the p-type Al_zGaN to form a p-type Al_zGaN cap, wherein forming a gate includes forming the gate on the p-type Al_zGaN cap.

4. The method of claim **3**, wherein forming the channel layer and forming the Al_xGaN layer on the channel layer forms a region of a first 2DEG charge, the method further comprising forming a layer surrounding the p-type Al_zGaN cap, the layer surrounding the p-type Al_zGaN cap and the channel layer together having a net 2DEG charge that is greater than the first 2DEG charge.

5. The method of claim **4**, wherein forming a layer surrounding the p-type Al_zGaN cap includes forming a layer of Al_yGaN, wherein $y<x$.

6. The method of claim **3**, wherein forming a cap layer of p-type Al_zGaN includes forming the cap layer to have a thickness of at least 50 Angstroms, with $0<z<1$.

7. The method of claim **1**, wherein forming a GaN channel layer comprises forming a channel layer having a thickness less than 300 Angstroms.

8. The method of claim **1**, wherein forming a GaN channel layer comprises forming a channel layer having a thickness about 50 Angstroms.

9. The method of claim **1**, wherein the device has a 2DEG charge that is depleted under the gate and has an internal barrier that is greater than 0.5 eV.

10. The method of claim **1**, wherein the channel layer is Al_zGaN, $0.05<z<0.15$.

11. The method of claim **1**, wherein forming the cap layer includes forming a multi-compositional cap layer, wherein a first layer of the cap layer comprises Al_xGaN and a second layer of the cap layer comprises of Al_yGaN, wherein the second layer is formed prior to the first layer being formed and $y>x$.

12. The method of claim **11**, further comprising:
- etching the multi-compositional cap layer to form a multi-compositional cap; and
- forming a layer of GaN surrounding the multi-compositional cap.

13. The method of claim **11**, wherein the multi-compositional cap layer changes from Al_xGaN to Al_yGaN in a continuous or discontinuous manner.

14. The method of claim **1**, wherein the carrier layer is thermally conducting and electrically insulating.

15. The method of claim **1**, wherein removing the substrate includes using laser liftoff, lapping, wet etching or dry etching.

16. The method of claim **1**, further comprising plasma treating a portion of an N-face that corresponds to a location in which the gate is subsequently formed.

17. The method of claim **1**, wherein:
- the channel layer and the layer of Al_xGaN form a heterostructure with a resulting 2DEG region in the channel layer, and the method further comprises implanting ions in an access region to increase net 2DEG charge.

18. The method of claim **1**, wherein the device has an access region, the method further comprising doping the access region by thermal diffusion of donor species.

19. The method of claim **1**, further comprising passivating an N-face layer after the N-face layer is exposed.

20. The method of claim **1**, further comprising forming an AlN layer on the channel layer prior to forming the layer of Al_xGaN.

21. The method of claim **1**, further comprising selectively doping an access region in the channel layer.

22. The method of claim **21**, wherein the doping includes thermal diffusion of donor species.

23. The method of claim **1**, further comprising forming a dielectric layer on a surface of an access region to form a pinning layer.

24. The method of claim **1**, wherein the sacrificial layer contains an etch stop layer.

25. A normally off III-nitride HEMT device, comprising:
- a gate;
- a source and a drain; and
- an access region formed of a III-nitride material between either the source and the gate or the drain and the gate, wherein the access region sheet resistance is less than 750 ohms/square;
- wherein the device has an internal barrier under the gate of at least 0.5 eV when no voltage is applied to the gate; and
- the device is capable of supporting a 2DEG charge density under the gate of greater than $1\times10^{12}/cm^2$ in the on state.

26. The device of claim **25**, wherein the device is capable of blocking at least 600 V.

27. The device of claim **26**, wherein the device has an on-resistance of less than 10 mohm-cm^2.